General-Purpose Code Acceleration with Limited-Precision Analog Computation

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ISCA 2014
How to use analog circuits for accelerating programs written in conventional languages?

1) Neural transformation
   [Esmaeilzadeh et. al., MICRO 2012]

2) Analog neurons

3) Compiler-circuit co-design
Challenges

- Analog circuits are mainly single function
- Instruction control cannot be analog
- Storing intermediate results in analog domain is not effective
- Analog circuits have limited operational range

1) **Neural transformation**

2) Analog neurons

3) Compiler-circuit co-design
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1) Neural transformation
2) Analog neurons
3) Compiler-circuit co-design
1st Design Principle

Neural Transformation
Neural Transformation

A-NPU acceleration

Source Codes

Common Intermediate Representation

Acceleration

CPU

A-NPU

Code 1

Code 2

Code 3

Code 4

Code 5

Code 6

…

Neural Representation

+ 

x
2nd Design Principle

Analog Neurons
Analog Neurons for Accelerated Computation

\[
y = \text{sigmoid}(\sum (x_i w_i))
\]

\[
y \approx \text{sigmoid}(\sum (I(x_i) R(w_i)))
\]
Mixed-signal A-NPU
Limitations of Analog Neuron

Limited range of operation (e.g. 600mV)

Margins for noise resiliency (2-3 mV)

Limited Bit-width

Topology Restriction

Circuit Non-idealities (e.g., Sigmoid)
3rd Design Principle

Compiler-Circuit Co-design
Digital Compilation Workflow

- Source Code
  - Programmer
  - Source Code + Annotations
  - Compiler + Training Algorithm
  - Accelerator Config
  - Instrumented Binary
  - D-NPU
  - CORE

Programming (Profiling, Training, Code Generation) → Compilation → Execution
Analog Compilation Workflow

Source Code

Programmer

Source Code + Customized Training Algorithm

Compiler

Accelerator Config

Instrumented Binary

Limited Bit-Width Topology Restriction Circuit Non-idealities

A-NPU

CORE

17
(1) Training with Limited Bit-width

Limited-Precision Network

Train a fully-precise neural network

Input the training data to the discretized neural network

Calculate the output error from the limited-precision neural network

Back propagate the error through the fully-precise neural network

Fully-Precise Network

Continuous-Discrete Learning Method (CDLM), E. Fiesler, 1990
(2) Training with topology restrictions and non-idealities

1) **Robust** to the topology restrictions

2) Tolerate a more shallow sigmoid activation steepness over all applications

Resilient Back Propagation (RPROP), M. Riedmiller, 1993
Measurements

Signal Processing, Robotics, 3D Gaming, Financial Analysis, Compression, Machine Learning, Image Processing

**Analog A-NPU with 8 Analog Neurons**
- Transistor-Level HSPICE Simulation
- Predictive Technology Models (PTM), 45nm
- Vdd: 1.2 V, f: 1.1 GHz

**Digital Components**
- Power Models: McPAT, CACTI, and Verilog

**Processor Simulator**
- Marssx86 Cycle-Accurate Simulation
- Intel Nehalem-like 4-wide/5-issue OoO processor
- Technology: 45 nm, Vdd: 0.9 V, f: 3.4 GHz
Ranges from 0.8× to 24.5× with Analog NPU
1.2× increase in application speedup with Analog over Digital NPU
Energy Savings

Energy saving with Analog NPU is very close to ideal case (6.5x)
Quality loss is below 10% in all cases but one
Based on application-specific quality metric
What is left?

3% Energy Reduction

46% Speedup

We can not reduce the energy of the computation much more.
Kirchhoff's Law

\[ I_{out} = I_0 + I_1 + I_2 \]

Ohm's Law

\[ V_o = I(x_n) \cdot R(w_n) \]

Saturation Property of Transistors

Quality Degradation: Avg. 8.2%, Max. 19.7%
It is still the beginning...

1) **Broad applicability** of the analog computation

2) Prototyping and integrating A-NPU within **noisy** high performance processors

3) Reasoning about the **acceptable level of error** at the programming level
Backup Slides
## Area Breakdown

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A-NPU</strong></td>
<td></td>
</tr>
<tr>
<td>8x8-bit DAC</td>
<td>3,096 T</td>
</tr>
<tr>
<td>8xResistor Ladder (8-bit weights)</td>
<td>4,096 T + 1 KΩ (≈ 450 T)</td>
</tr>
<tr>
<td>8xDifferential Pair</td>
<td>48 T</td>
</tr>
<tr>
<td>I-to-V Resistors</td>
<td>20 KΩ (≈ 30 T)</td>
</tr>
<tr>
<td>Differential Amplifier</td>
<td>244 T</td>
</tr>
<tr>
<td>8-bit ADC</td>
<td>2,550 T + 1KΩ (≈ 450)</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>≈ 10,964 T</td>
</tr>
<tr>
<td><strong>D-NPU</strong></td>
<td></td>
</tr>
<tr>
<td>8x8-bit multiply-adds</td>
<td>≈ 56,000 T</td>
</tr>
<tr>
<td>8-bit Sigmoid lookup table</td>
<td>16,456 T</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>≈ 72,456</td>
</tr>
</tbody>
</table>

6.6x fewer transistors in the analog neuron implementation
## Power Breakdown

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Percentage of total power</th>
</tr>
</thead>
<tbody>
<tr>
<td>A-NPU</td>
<td></td>
</tr>
<tr>
<td>SRAM-accesses</td>
<td>13%</td>
</tr>
<tr>
<td>DAC-Resistor Ladder-Diff Pair-Sum</td>
<td>54%</td>
</tr>
<tr>
<td>Sigmoid-ADC</td>
<td>33%</td>
</tr>
</tbody>
</table>

Power numbers vary with applications
Applications

**Signal Processing**
- **fft**
  - 34 x86 instructions
  - 67.4% dynamic instructions
  - 1 → 4 → 4 → 2
  - Error: 4.1%

**Compression**
- **jpeg**
  - 1,257 x86 instructions
  - 56.3% dynamic instructions
  - 64 → 16 → 8 → 64
  - Error: 8.4%

**Robotics**
- **inversek2j**
  - 100 x86 instructions
  - 95.9% dynamic instructions
  - 2 → 8 → 2
  - Error: 9.4%

**Machine Learning**
- **kmeans**
  - 26 x86 instructions
  - 29.7% dynamic instructions
  - 6 → 8 → 4 → 1
  - Error: 7.3%

**3D Gaming**
- **jmeint**
  - 1,079 x86 instructions
  - 95.1% dynamic instructions
  - 18 → 32 → 8 → 2
  - Error: 19.7%

**Image Processing**
- **sobel**
  - 88 x86 instructions
  - 57.1% dynamic instructions
  - 9 → 8 → 1
  - Error: 5.2%

**Financial**
- **blackscholes**
  - 309 x86 instructions
  - 97.2% dynamic instructions
  - 6 → 8 → 8 → 1
  - Error: 10.2%
Speedup with A-NPU over 8-bit D-NPU

3.3× geometric mean speedup
Ranges from 1.8× to 15.2×
Energy savings with A-NPU over 8-bit D-NPU

12.1× geometric mean speedup
Ranges from 3.7× to 82.2×
Dynamic Instruction Reduction

Percentage of Instructions Subsumed

- blackscholes: 100%
- fft: 70%
- inversek2j: 90%
- jmeint: 80%
- jpeg: 60%
- kmeans: 30%
- sobel: 50%
- geometric mean: 66.4%
Speedup with A-NPU acceleration

3.7× geometric mean speedup
Ranges from 0.8× to 24.5×
Energy savings with A-NPU acceleration

Energy savings with A-NPU acceleration:

- blackscholes: $51.2 \times$
- fft: $30.0 \times$
- inversek2j: $17.8 \times$

All benchmarks benefit from A-NPU acceleration:

- jpeg
- kmeans
- sobel
- geomean

6.3× geometric mean energy reduction
All benchmarks benefit